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Atty. Dkt. No. 029471-0168

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Hiroyuki TAKAHASHI, et al.

Title: SEMICONDUCTOR MEMORY DEVICE AND SEMICONDUCTOR MEMORY DEVICE CONTROL METHOD

Appl. No.: 10/507,117

Filing Date: 9/10/2004

Examiner: Hur, Jung H.

Art Unit: 2824

Confirmation Number: 4725

RESPONSE TO RESTRICTION REQUIREMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the restriction requirement set forth in the Office Action mailed May 03, 2006, Applicants hereby elect Group I, including claims 1-38 and 41-48, for examination, with traverse.

Applicants believe that at least claims 39 and 40 should be examined along with the Group I claims, because of their dependency on claims from Group I. Specifically, claim 39 recites "wherein the semiconductor device comprises the delay circuit according to claim 13 as said delay circuit", where claim 13 is a Group I claim. Claim 40 depends from claim 3, another Group I claim.

Respectfully submitted,

Date May 31, 2006

By _____

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